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To carry the high current out of the silicon, additional metal has to be placed on top of the tungsten layer. This may be done by many methods including plating, evaporation and sputtering. If plating is utilized, and/or lead based plating, the new metal layer plates out preferentially on tungsten requiring no metal etching afterwards. If sputtering or evaporation of aluminum is used, more steps are needed since these deposition techniques are typically not sufficiently selective.

As shown in FIG. 6B, as inherently effected by the selective depositions, the metal and/or silicide are formed co-extensively over the polysilicon surface. --

On page 14, after line 28, insert as follows:

-- Further to such completion and as incorporated herein by reference to U.S. Pat. No. 5,262,336, for example, a second layer of metal is deposited in gate pad regions of the gate contact layer in isolation from the source pads over a passivation layer. Additionally, a double or a triple layer of metal can be deposited in the source bonding pad and bus areas. This measure improves current handling capability, links the source metal areas together in isolation from the gate pads and busses.

new method 132
for non-trench type MOSFET only
Referencing FIGS. 6C (FIG. 16B of U.S. Pat. No. 5,262,336), a layer 272 can be applied on top of areas 230 and 228. This layer may be a resin such as photoresist or any number of other compounds such as polyimide or spin-on glass. Layer 272 is applied to assist surface planarization and may be applied using spin, spray, or roll-on techniques familiar to one skilled in the art to give the preferred coating. Planarization can be done by conventional techniques familiar to one skilled in the art, such as plasma etching, ion milling, reactive ion etching, or wet chemical etching. The underlying layers 228 and 230, of the source and gate respectively, remain covered and thus unetched. Next, artifacts 274 are etched away, and any metal extending downward along the sidewalls can be removed by continuing the etch. In some procedures, layer 272 is then removed by any conventional means. However, if layer 272 is a material that can remain on the device surface, such as glass, its removal is not necessary. A passivation layer is then deposited, as is commonly done.

OK
guard ring structure of a planar type MOSFET
In accordance with an exemplary embodiment of the present invention, the passivation layer comprises at least one of the group consisting of oxide, nitride, glass and phosphosilicate glass (PSG), e.g., as set forth in incorporated 5,262,336 (e.g., at column 24, line 61 to column 27, line 50). --